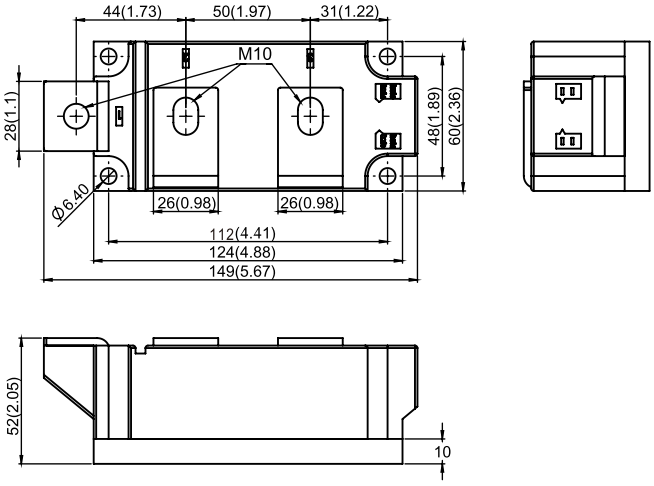
Thyristor/Diode and Thyristor/Thyristor, 500A
(SUPER MAGN-A-PAK Power Modules)

SUPER MAGN-A-PAK (Vishay)



All dimensions in millimeters(inches)

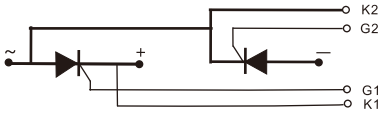
FEATURES

- High voltage
- Electrically isolated by DBC ceramic (Al_2O_3)
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- High surge capability
- Modules uses high voltage power thyristor/diodes in two basic configurations
- Simple mounting
- UL approved file E320098
- Compliant to RoHS
- Designed and qualified for multiple level

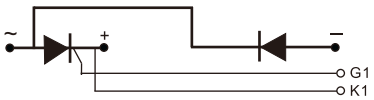
RoHS COMPLIANT

APPLICATIONS

- DC motor control and drives
- Battery charges
- Welders
- Power converters
- Lighting control
- Heat and temperature control
- Ups



NKT



NKH

PRODUCT SUMMARY	
$I_{T(AV)}$	500 A

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUE	UNITS
$I_{T(AV)}$	85 °C	500	A
$I_{T(RMS)}$	85 °C	785	A
I_{TSM}	50 Hz	16000	A
	60 Hz	16800	A
I^2t	50 Hz	1280	kA^2s
	60 Hz	1167	kA^2s
$I^2\sqrt{t}$		12800	$kA^2\sqrt{s}$
V_{DRM} / V_{RRM}	Range	400 to 1600	V
T_J	Range	-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125 °C mA
NKT500/xx-1 NKH500/xx-1	04	400	500	40
	08	800	900	
	10	1000	1100	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

FORWARD CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave ,50Hz			500	A
					85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave ,50Hz ,T_C = 85°C			785	A
Maximum peak, one-cycle, on-state non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial T_J = T_J maximum	16000	
		t = 8.3 ms			16800	
Maximum I^2t for fusing	I^2t	t = 10 ms			1280	kA^2s
		t = 8.3 ms			1167	
		t = 10 ms	100%V_{RRM} reapplied		896	
		t = 8.3 ms			818	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			12800	$kA^2\sqrt{s}$
Maximum on-state voltage drop	V_{TM}	I_{TM} = 1500A, T_J = 25 °C, 180° conduction			1.7	V
Maximum forward voltage drop	V_{FM}	I_{FM} = 1500A, T_J = 25 °C, 180° conduction			1.4	
Maximum holding current	I_H	Anode supply = 12 V initial I_T = 30 A, T_J = 25 °C			300	mA
Maximum latching current	I_L	Anode supply = 12 V resistive load = 1 Ω Gate pulse: 10 V, 100 µs, T_J = 25 °C			500	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical delay time	t_d	T_J = 25 °C ,gate current = 1A, dI_g/dt = 1 A/µs V_d = 0.67 V_{DRM}	2	µs
Typical rise time	t_r		4	
Typical tum-off time	t_q	I_{TM} = 750A ; dI/dt = -60 A/µs ; T_J = T_J maximum, V_R = 50V ; dV/dt = 20V/µs ; gate 0V ,100Ω	200	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	T_J = 125°C	40	mA
RMS isolation Voltage	V_{ISO}	50 Hz, circuit to base, all terminals shorted, 25°C, 1s	3500	V
Critical rate of rise of off-state voltage	dV/dt	T_J = T_J maximum, linear to V_D = 80% V_{DRM}	1000	V/µs

TRIGGERING					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**VALUES**	**UNITS**
Maximum peak gate power	P_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		10	W
Maximum average gate power	$P_{G(AV)}$	f = 50 Hz, $T_J = T_J$ maximum		3	
Maximum peak gate current	I_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		3	A
Maximum peak positive gate voltage	$+V_{GM}$			20	V
Maximum peak negative gate voltage	$-V_{GM}$			5.0	
Maximum required DC gate voltage to trigger	V_{GT}	T_J = 25 °C	Anode supply = 12 V, resistive load; R_a = 1 Ω	2	
Maximum required DC gate current to trigger	I_{GT}			200	mA
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, 67% V_{DRM} applied		0.25	V
Maximum gate current that will not trigger	I_{GD}			10	mA
Maximum rate of rise of turned-on current	dI/dt	$T_J = T_J$ maximum, I_{TM} = 400A rated V_{DRM} applied		1000	A/µs

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
junction operating and storage temperature range	T_J, T_{stg}		- 40 to 125	°C
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.065	°C/W
Typical thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface, smooth , flat and greased	0.01	
Mounting torque ± 10 % — SMAP to heatsink , M6		A mounting compound is recommended and the torque should be rechecked after a period of about 3 hours to allow for the spread of the compound.	6 to 8	N.m
Mounting torque ± 10 % — busbar to SMAP , M10			12 to 15	
Approximate weight			1800	g
			63.5	oz.
Case style			Vishay SUPER MAGN-A-PAK	

ORDERING INFORMATION TABLE

Device code

NKT	500	/	16	—	1
①	②		③		④

1 - Module type: NKT for (Thyristor + Thyristor) module
NKH for (Thyristor + Diode) module

2 - Current rating: $I_{T(AV)}$

3 - Voltage code x 100 = V_{RRM}

4 - "1" for Vishay super MAP outline

Fig.1 On-state current vs. voltage characteristics

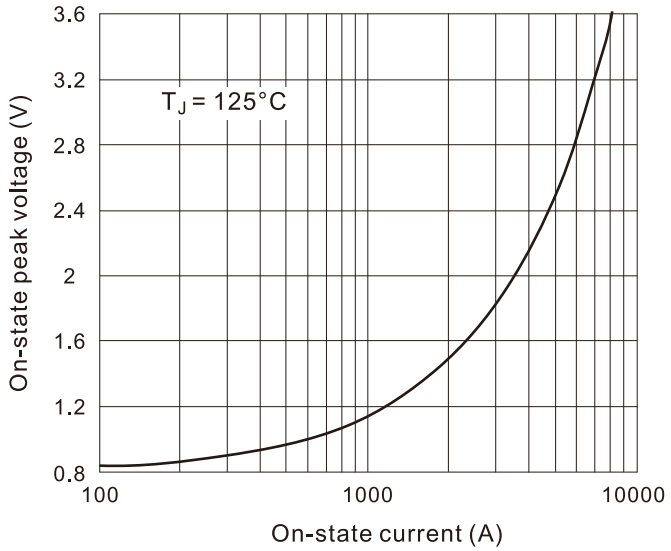


Fig.2 Transient thermal impedance(junction-case)

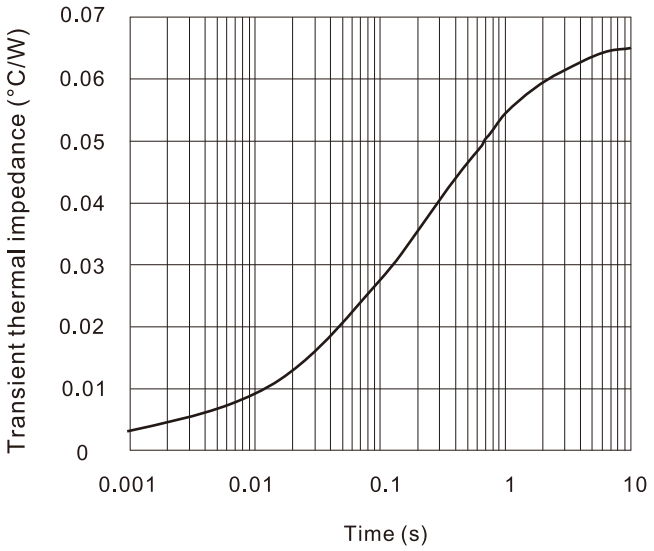


Fig.3 Power consumption vs. average current

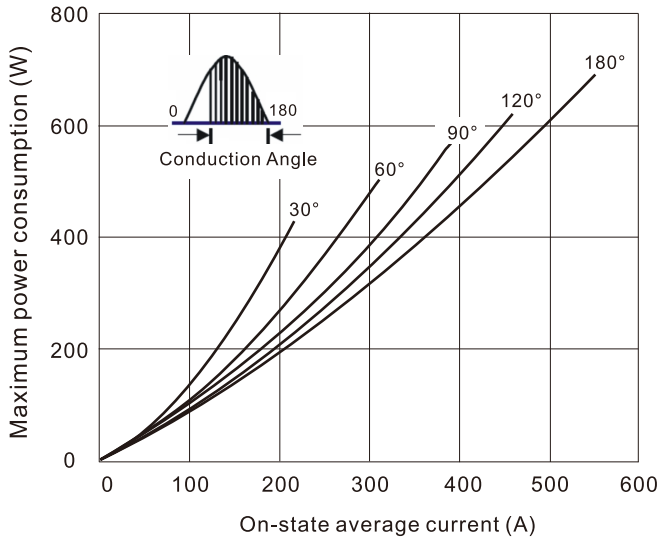


Fig.4 Case temperature vs. on-state average current

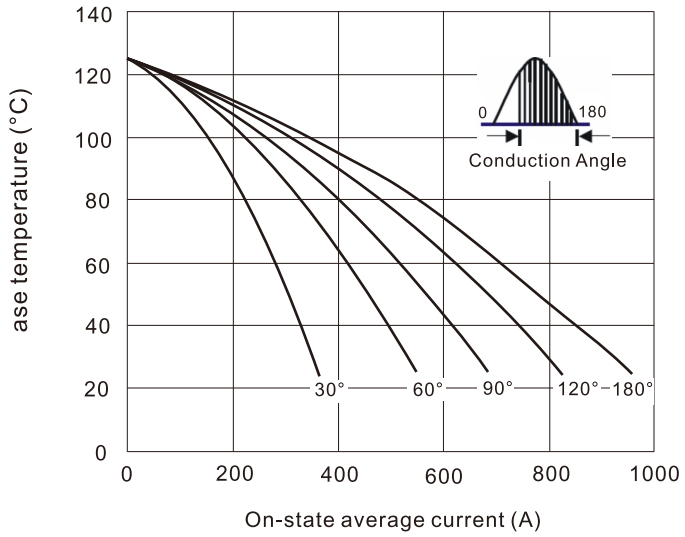


Fig.5 On-state surge current vs cycles

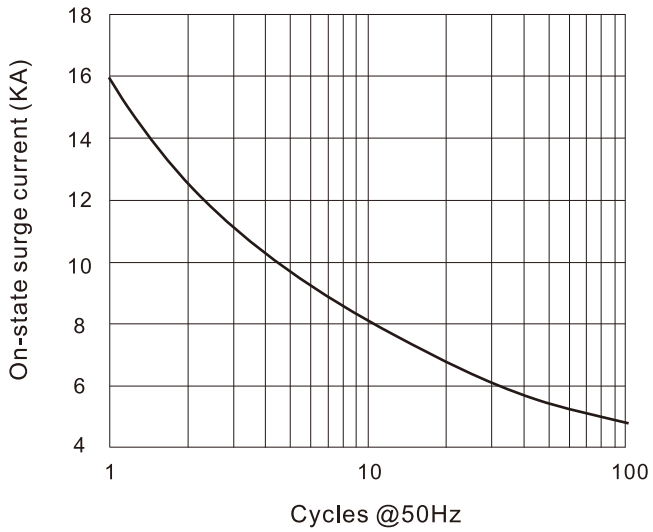


Fig.6 I^2t characteristics